Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (previously presented) A program circuit comprising:

a comparator for comparing output data of a data input buffer with output data of a sense amplifier bit by bit, and for outputting a re-program operation signal if the data are different from each other;

a data latch circuit for latching the comparing results of the output data of said data input buffer and the output data of said sense amplifier;

a control circuit for generating a high voltage for receiving the output data of said data input buffer and the data latched at said data latch circuit, respectively, and for outputting a signal for applying a program bias voltage to a memory cell which has not been completely programmed in response to a power-up reset signal and program state signal.

2. (previously presented) The program circuit as claimed in claim 1, wherein said comparator includes a plurality of exclusive-NOR gates to which output data of said data input buffer and output data of said sense amplifier, respectively, and a NOR gate for logically combining the output signals of said exclusive-NOR gates.

3. (previously presented) The program circuit as claimed in claim 1, wherein said data latch circuit includes a plurality of flip-flops, each flip-flop having a data input terminal to which comparing results of the output data of said data input buffer and the output data of said sense amplifier, a clock signal input terminal to which a program state signal and a reset signal input signal to which power-up reset signal/program state signal/read mode signals are inputted.

4. (previously presented) The program circuit as claimed in claim 1, wherein said control circuit for generating a high voltage includes a plurality of NOR gates to which output data of said data latch circuit and a power-up reset signal are inputted, respectively; a

plurality of inverters to which output data of said data input buffer is inputted; and a plurality of NAND gates to which the output signals of said NOR gates, the output signals of said inverters and the program state signal are inputted, respectively.

5. (previously presented) The program circuit as claimed in claim 1, wherein said comparator includes eight exclusive-NOR gates to compare the output data of said data input buffer and the output data of said sense amplifier.

6-16. (canceled)

17. (currently amended) A non-volatile memory device, comprising:

a plurality of memory cells;

an input component coupled to the memory cells and configured to program first information into the memory cells; and

a given circuit configured to reprogram only the memory cells that have not been properly programmed, ~~The non-volatile memory device of claim 16,~~ the ~~primary~~ given circuit including:

a first circuit to determine if the first information has been properly programmed into the memory cells; and

a second circuit to transmit a signal to initiate reprogramming of any memory cells that has not been properly programmed.

18. (currently amended) The non-volatile memory device of claim ~~16~~17, wherein the first information is no more than four bits of data and are programmed in parallel.

19. (currently amended) The non-volatile memory device of claim ~~16~~17, wherein the first information is no more than two bits of data and are programmed in parallel.

20. (previously presented) A semiconductor device, comprising:

a plurality of memory cells;

an input component coupled to the memory cells and configured to program the memory cells;

a comparator to determine whether first information of the input component has been properly programmed into the memory cells, the comparator having a logic gate to output a first signal to indicate whether or not a reprogramming operation is needed, wherein the first information is N bits of data; and

a controller coupled to the comparator and configured to output a second signal to initiate reprogramming of M number of the memory cells, where M is less than N.

21. (previously presented) The device of claim 20, wherein the comparator compares the first information of the input component with second information read from the memory cells.

22. (previously presented) The device of claim 21, wherein N is eight and the input component is configured to transmit a byte of information at a time to the memory cells.

23. (previously presented) The device of claim 22, wherein the comparator includes:

a plurality of XNOR gates having first and second input ports, the first input ports being configured to receive the first information and the second input ports being configured to receive the second information, wherein outputs of the XNOR gates indicate whether the first information and the second information are the same.

24. (previously presented) The device of claim 23, wherein the comparator includes N number of the XNOR gates.

25. (previously presented) The device of claim 23, wherein the comparator further includes:

a logic gate coupled to the outputs of the XNOR gates, the logic gate configured to output the second signal.

26. (previously presented) The device of claim 23, further comprising:

a sense amplifier coupled to the memory cells, wherein the sense amplifier provides the second information to the second input ports of the XNOR gates.

27. (previously presented) The device of claim 26, further comprising:

a latch configured to receive information relating to the first information of the input component.

28. (previously presented) The device of claim 27, wherein the latch receives the outputs of the XNOR gates.

29. (previously presented) The device of claim 28, wherein the latch includes N number of flip-flops to receive the outputs of the XNOR gates.

30. (previously presented) The device of claim 27, wherein the information received by the latch is the first information of the input component.

31. (previously presented) The device of claim 27, wherein an output of the latch is transmitted to the controller.

32. (previously presented) The device of claim 31, wherein the first information of the input component is transmitted to the controller.

33. (previously presented) The device of claim 32, wherein the first information and the output of the latch are eight bits of data, respectively, where the controller outputs eight signals in response to receipt of the first information and the output of the latch, the eight signals having one or more signals of first type to initiate reprogramming of corresponding one or more memory cells that have not been properly programmed and one or more of signals of second type to disable reprogramming of corresponding one or more memory cells that have been properly programmed.

34. (previously presented) The device of claim 20, wherein N is 2.

35. (previously presented) The device of claim 20, wherein N is one selected from one of the following: 32, 16 and 8.

36. (previously presented) The device of claim 20, wherein M corresponds to a number of the memory cells that have not been properly programmed.

37. (previously presented) The device of claim 36, wherein M is proportional to the number of the memory cells that have not been properly programmed.

38. (previously presented) The device of claim 36, wherein M is equal to the number of the memory cells that have not been properly programmed.

39. (previously presented) The device of claim 20, wherein N is 4.

40. (previously presented) The device of claim 39, wherein M is 2.

41. (previously presented) A non-volatile semiconductor device, comprising:

a plurality of memory cells;

a sense amplifier coupled to the memory cells to read information written into the memory cells;

an input data buffer coupled to the memory cells and configured to transmit N bits of information at a time into the memory cells;

a comparator having a plurality of logic gates to compare bit-by-bit first information of the input data buffer with second information of the sense amplifier and output a reprogram operation signal if the first information and the second information are different;

a data latch circuit coupled to outputs of one or more of the logic gates of the comparator; and

a controller having a plurality of logic gates and being configured to receive the first information of the input data buffer and outputs of the data latch circuit, and output a signal for applying a program bias voltage to any memory cell that has not been properly programmed.

42. (previously presented) The non-volatile device of claim 41, wherein the plurality of logic gates of the controller include a first set of logic gates of N numbers corresponding to the N bits of information programmed into the memory cells, the first set of logic gates being configured to output a high voltage signal for any bit of information that has not been properly programmed into the memory cells.

43. (previously presented) The non-volatile device of claim 42, wherein the signal for applying the program bias voltage is a low voltage signal.

44. (previously presented) A non-volatile semiconductor device, comprising:

a plurality of memory cells;

a sense amplifier coupled to the memory cells;

an input data buffer coupled to the memory cells and configured to write N bits of information at a time into the memory cells;

a comparator having N number of XNOR gates corresponding to the N bits of information being written into the memory cells, the comparator being configured to compare bit-by-bit N bits of first information of the input data buffer with N bits of second information of the sense amplifier and output a rewrite operation signal if any bit of the first information and the second information is different from each other;

a data latch circuit coupled to the comparator to receive outputs of the XNOR gates; and

a controller having a plurality of logic gates and being configured to receive the first information of the input data buffer and outputs of the data latch circuit, and configured to output a signal for applying a bias voltage to any memory cell that has not been properly written,

wherein the plurality of logic gates of the controller include a first set of logic gates of N numbers corresponding to the N bits of information written into the memory cells, the first set of logic gates being configured to output a high voltage signal for any bit of information that has not been properly written into the memory cells.

45-49. (canceled)